CLAIMS

1. A transistor overlying a substrate, the transistor comprising:

a first current handling terminal;

a second current handling terminal;

a plurality of channels overlying the substrate, wherein each of the plurality of channels are electrically coupled to the first current handling terminal and the second current handling terminal, and wherein at least one of the plurality of channels overlies another one of the plurality of channels, wherein the first current handling terminal is comprised of a first substantially homogenous crystal lattice, the second current handling terminal is comprised of a second substantially homogenous crystal lattice, and the plurality of channels is comprised of a third substantially homogenous crystal lattice; and

a control terminal proximate to the plurality of channels for modulating the plurality of channels through a dielectric.

2. The transistor of claim 1 wherein the control terminal is shaped to fully loop around at least one channel.

3. The transistor of claim 2 wherein the plurality of channels form a vertical stack.

4. The transistor of claim 1 wherein the plurality of channels further comprise at least two channels of differing thickness.

5. The transistor of claim 1 wherein at least two of the plurality of channels are separated from an adjacent channel by a different amount.

6. The transistor of claim 1 wherein the plurality of channels form a vertical stack.

7. The transistor of claim 1 wherein each of the first and second current handling terminals have a width substantially equal to a first value and each of the plurality of channels has a width substantially equal to a second value, wherein the first value is greater than the second value.

8. The transistor of claim 1 wherein the plurality of channels are physically separated at least by portions of a control terminal material.

9. An integrated circuit comprising:

a substrate; and

a transistor overlying the substrate, the transistor comprising:

a first channel overlying the substrate;

a first portion of a gate electrode overlying the first channel;

a second channel overlying the first portion of the gate electrode;

a second portion of the gate electrode overlying the second channel and connecting to the first portion of the gate electrode;

a first current handling electrode connected to the first channel and the second channel; and

a second current handling electrode connected to the first channel and the second channel.

10. The transistor of claim 9 wherein each of the first current handling electrode and the second current handling electrode has a minimum width that is greater than a maximum width of each of the first channel and the second channel.

11. The transistor of claim 9 further comprising:

a gate dielectric material disposed between each of the first channel and the second channel and the gate electrode.

12. The transistor of claim 9 wherein the first portion of the gate electrode is connected to the second portion of the gate electrode to form a loop around the second channel.

13. A method of fabricating a vertical multiple-channel FET device comprising:

providing an integrated circuit substrate;

providing at least two layers of a first composition having a first etch property;

providing at least one layer of a second composition having a second etch property, wherein the at least two layers of the first composition and the at least one layer of the second composition are formed to have a substantially homogenous crystallinity and wherein the at least two layers of the first composition are separated by the at least one layer of the second composition;

forming a blocking layer over the at least two layers of the first composition and the at least one layer of the second composition;

patterning the blocking layer to define placement of a first current electrode region, a second current electrode region and a plurality of channels;

etching exposed portions of the at least two layers of the first composition and the at least one layer of the second composition to form the first current electrode region, the second current electrode region and channel regions extending from the integrated circuit substrate;

further etching the at least one layer of the second composition to remove said at least one layer of the second composition and form the plurality of channels comprised of the first composition and located above and below any removed portion of the at least one layer of the second composition;

depositing a control electrode dielectric around each of the plurality of channels;

depositing control electrode material around the control electrode dielectric;

selectively masking and etching the control electrode material to form a control electrode on top, bottom and sidewall surfaces of at least one of the plurality of channels; and

forming a spacer to isolate the control electrode material from the first current electrode region and the second current electrode region.

14. The method of claim 13 wherein providing the at least two layers of a first composition having a first etch property comprises forming the at least two layers of the first composition by epitaxially growing the at least two layers of the first composition.

15. The method of claim 13 further comprising:

forming additional material overlying areas adjacent the control electrode and the spacer to reduce resistance of the first current electrode region and the second current electrode region of the vertical multiple-channel FET device.

16. The method of claim 13 further comprising:

etching the at least one layer of the second composition at the first current electrode region and the second current electrode region; and

forming additional material at areas not covered by the control electrode and the spacer to reduce resistance of the first current electrode region and the second current electrode region of the vertical multiple-channel FET device.

17. The method of claim 13 further comprising selecting composition of the integrated circuit substrate to be one of the group consisting of silicon, silicon on insulator, silicon on sapphire, and silicon on nitride.

18. The method of claim 13 further comprising forming the integrated circuit substrate as a plurality of layers, one of the plurality of layers of the integrated circuit substrate having the first composition.

19. The method of claim 13 further comprising providing the integrated circuit substrate as a silicon-on-insulator (SOI) bonded wafer having a silicon layer which functions as one of the at least two layers of the first composition.

20. The method of claim 13 further comprising providing the at least two layers of a first composition and the at least one layer of a second composition by using at least one of the group of processes consisting of epitaxial growth, atomic layer deposition, and molecular beam epitaxy.

21. The method of claim 13 further comprising selecting the first composition from one of the group consisting of silicon, germanium, silicon germanium and silicon germanium carbon and selecting the second composition from one of silicon, germanium, silicon germanium and silicon germanium carbon.

22. The method of claim 13 further comprising selecting the first composition from one of the group consisting of gallium arsenide, gallium nitride and indium phosphide, and selecting the second composition from one of the group consisting of gallium arsenide, gallium nitride and indium phosphide.

23. The method of claim 13 further comprising forming the blocking layer from one of the group consisting of photoresist, nitride, oxide, and organic anti-reflective coating.

24. The method of claim 13 wherein the further etching of the at least one layer of the second composition to remove said at least one layer of the second

composition and form the plurality of channels further comprises etching to create a height of each of the plurality of channels to be less than a length of the control electrode.

25. The method of claim 13 further comprising:

blocking the control electrode by using a blocking layer before etching the at least one layer of the second composition to remove the at least one layer of the second composition at least at the plurality of channels.